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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/827,248	04/04/2001	David R. Hembree	MI22-1684\US	2645
21567	7590	09/14/2004	EXAMINER	
WELLS ST. JOHN P.S. 601 W. FIRST AVENUE, SUITE 1300 SPOKANE, WA 99201			NGUYEN, VINH P	
			ART UNIT	PAPER NUMBER
			2829	

DATE MAILED: 09/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/827,248	Applicant(s) HEMBREE, DAVID R.	
	Examiner VINH P NGUYEN	Art Unit 2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 16 July 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 89-133 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 98-107 is/are allowed.
- 6) ☒ Claim(s) 89-97, 108-113, 115-123, 131, 133 is/are rejected.
- 7) ☒ Claim(s) 114, 126-130, 132 and 134-136 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>0704</u> . | 6) <input type="checkbox"/> Other: _____ |

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1. The disclosure is objected to because of the following informalities: “calibration wafer” is not well defined in the specification. Is it different from a regular wafer?

Appropriate correction is required.

2. Claims 126-130,132 are objected to because of the following informalities:

In claim 126, it is unclear what “a calibration wafer” is. Is it different from a regular wafer?

In claim 127, it is unclear what is meant by “originating the signals”. Furthermore, it is also unclear how this originating step is interrelated and associated with other steps recited in claim 89.

In claims 128-130, it is unclear what “a calibration workpiece”. Is it different from a regular workpiece?

In claim 132, it is unclear how “a production workpiece” is interrelated and associated with “workpiece” in claim 115. Is it different from “workpiece” in claim 115.

Appropriate correction is required.

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 89-97,108-113,115-123,125,131,133 are rejected under 35 U.S.C. 102(B) as being anticipated by Baker et al (Pat # 4,104,589).

As to claims 89-90,95,108,115-116,119 Baker et al disclose an for testing of semiconductor wafer as shown in figure 1 having a workpiece processing apparatus including a wafer holder (18) having circuitry (11,12,20,22) coupled to a wafer under test (not shown) and communicate signals intermediate the circuitry of the wafer (electrical contact regions on the bottom surface of the wafer) and the circuitry (11,12,20,22) of the holder . It is noted that the word “process” is not necessary related to a method of making but it is defined as a series of actions, changes, or functions bringing about a result, testing environment would be qualified for this definition. the term “process”. Furthermore, the limitation of “usable to form at least one semiconductor device” is an intended use, therefore this limitation is not given any patentable weight.

As to claims 91,109,122, the receiving of Baker et al is a wafer.

As to claim 93, it appears that during communication/contacting between the wafer and the holder includes communicating during the processing (testing).

As to claims 94, 112, it appears that the electrical coupling /circuitry (11,12,20,22) are qualified as “the intermediate member of the holder.

As to claims 96,113,123, the communicating signals (electrical signals obtained from making contact) are information.

As to claim 97, the communicating signals includes information regarding the process condition (testing condition). It is noted that the word “process” is not necessary related to a method of making, it is defined as a series of actions, changes, or functions bringing about a result, testing environment would be qualified for this definition. However the term “process”

As to claims 110,120,125, it appears that the coupling step of Baker et al includes the coupling the circuitry of the wafer and the circuitry of the workpiece/wafer holder “18” at a surface of the wafer and a surface of the workpiece/wafer holder “18” .

As to claims 111, 117, the step of coupling would include the step of contacting the circuitry of the wafer and the circuitry of the workpiece/wafer holder (18).

As to claim 115, the limitation of “adapted to form a semiconductor” is an intended use, therefore this limitation is not given any patentable weight.

As to claim 118, it appears that soon after the testing is done, the wafer is removed from the wafer holder and this removing step would include the step of breaking the coupling of the circuitry of the workpiece/wafer and the circuitry (11,12,20,22) of the workpiece processing apparatus.

As to claim 121, Baker et al teach that the step of supporting the workpiece/wafer under

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test within the workpiece processing apparatus (18,11,12,20,22) using a workpiece holder (18) and an intermediate member (11,12,20,22).

In claim 131, it appears that Baker et al expose the workpiece/wafer to process conditions (testing conditions). It is noted that the limitation of “configured to form the semiconductor device” is an intended use, therefore this limitation is not given any patentable weight.

As to claim 133, Baker et al teach that the receiving step uses circuitry of the workpiece processing apparatus (11,12,20,22,18) for receiving signals comprising information.

5. Claims 98-107 are allowable since the prior art fail to disclose a method of processing a workpiece having a combination steps of providing a first workpiece and a second workpiece, processing the first workpiece to form a semiconductor device, using intermediate member for communication between the second workpiece and the workpiece holder of the workpiece processing apparatus.


6. Claims 114,134-136 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The prior art fail to disclose signals information is related to process conditions, temperature at a plurality of different positions of a surface of the Workpiece of the workpiece processing apparatus.

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7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to VINH P. NGUYEN whose telephone number is (703) 305-4914.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-4900.


VINH P. NGUYEN
PRIMARY EXAMINER
ART UNIT 2829
09/08/04